

IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 3, line 4 is amended as follows:

*Wm Bn*  
*at* In accordance with the first aspect the present invention provides a parallel counter which is based on algebraic properties of symmetric functions. Each of the plurality of binary output bits is generated as a symmetric function of a plurality of binary input bits to a plurality of the binary output bits are each generated as a symmetric function of a plurality of a binary input bits. *>*